Data Sheet & Application Manual

Intelligent Gate Drivers

for IGBTs and Power MOSFETs

Description

The intelligent gate drivers of the IGD type series are single-channel drive components designed for IGBTs and power MOSFETs. They were developed specifically for the precise and reliable driving and protection of high-power modules, high-voltage modules, series and parallel circuits.

The IGD508EI/EN and IGD515EI/EN drivers are mutually pin-compatible and differ only in their driver power. The drive information and the status acknowledgement are transmitted via external fiber-optic links. The drivers contain an integrated DC/DC converter with a high isolation test voltage. Special logic functions allow the implementation of reliable series circuits with IGBTs or power MOSFETs.

Product Highlights

- ✔ Suitable for IGBTs and power MOSFETs
- ✔ Protect the power transistors
- ✔ Extremely reliable, long service life
- ✔ High gate current of ±1.5A to ±8A
- ✔ Electrical isolation 4000 Vac
- ✔ Series connection functions
- ✔ Monitoring of power supply and self-monitoring
- ✔ Switching frequency DC to MHz
- ✔ Duty cycle: 0... 100%
- ✔ Fiber-optic links make long drive cables possible
- ✔ Shorten development time

Applications

- ✔ Inverters
- ✔ Motor drive technology
- ✔ Traction
- ✔ Railroad power supplies
- ✔ Converters
- ✔ Power engineering
- ✔ Switch-mode power supplies
- ✔ Radiology and laser technology
- ✔ DC/DC converter
- ✔ Research
- ✔ RF generators and converters

Absolute Maximum Ratings

Parameter	Test conditions	min	max	Unit
Supply voltage V_{cc}	Pin 10 to Pin 9	-0,5	16	Vdc
Logic input voltage	All types (see note 5)		5	Vdc
Gate peak current I_{out}	IGD 506Ex Pin 25	-8	+8	A
	IGD 515xx Pin 25	-15	+15	A
Test voltage (50Hz/1min)	INxx to output stages		7500	Vac
Operating temperature	IGDxxxEN	0	+70	°C
	IGDxxxEI	-40	+85	°C
Storage temperature	All types	-45	+90	°C

Pin Designation

Pin	Desig.	Function	Pin	Desig.	Function
1	GND	Power supply GND	36	Cq	Acknowledgement pulse capacitor
2	GND	Power supply GND	35	SO	Status output signal
3	GND	Power supply GND	34	SDOSA	series-connected IGBT mode
4	GND	Power supply GND	33	INV	Inverse input
5		Not present	32	INPUT	Input signal from FOL
6		Not present	31	+5V	5V power supply for FOL
7		Not present	30	IGND	GND for FOL
8		Not present	29		Not present
9	GND	Power supply GND	28		Not present
10	Vcc	Power supply plus terminal	27		Not present
11		Not present	26		Not present
12		Not present	25	G	Gate driver output
13		Not present	24	COM	Virtual common
14		Not present	23	Cs	Blocking capacitor
15	NC	Not connected	22	E	Emitter / Source
16	NC	Not connected	21	REF	External reference
17	NC	Not connected	20	Cb	Blocking time capacitor
18	NC	Not connected	19	ME	V_{CE} measurement

Legend for terminal assignment:

Pins with the designation "not connected" are physically present but must not be connected to an electrical potential. Pins with the designation "not present" are not physically present.
The abbreviation "FOL" stands for Fiber-Optic Link.

Block Diagram

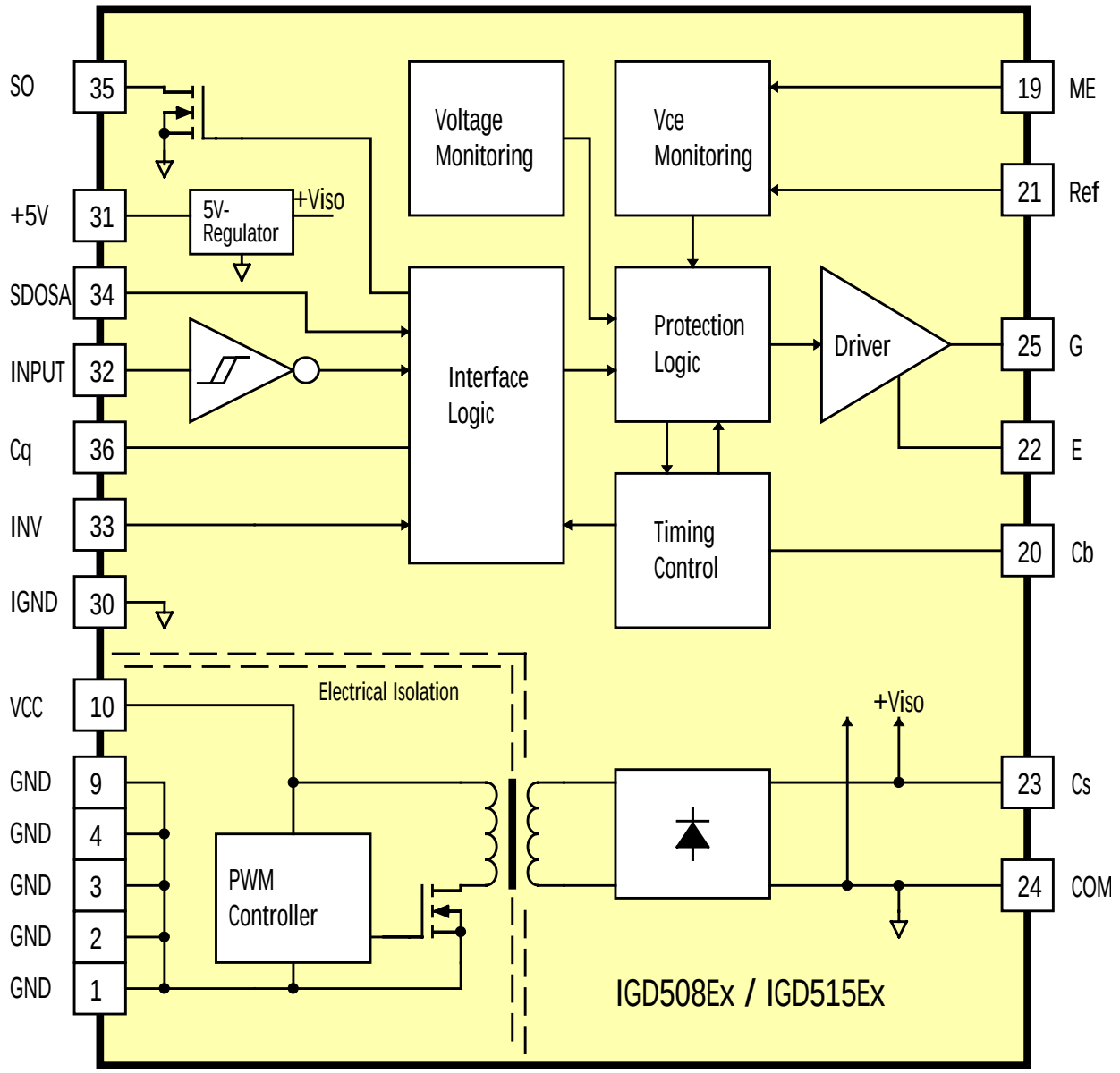
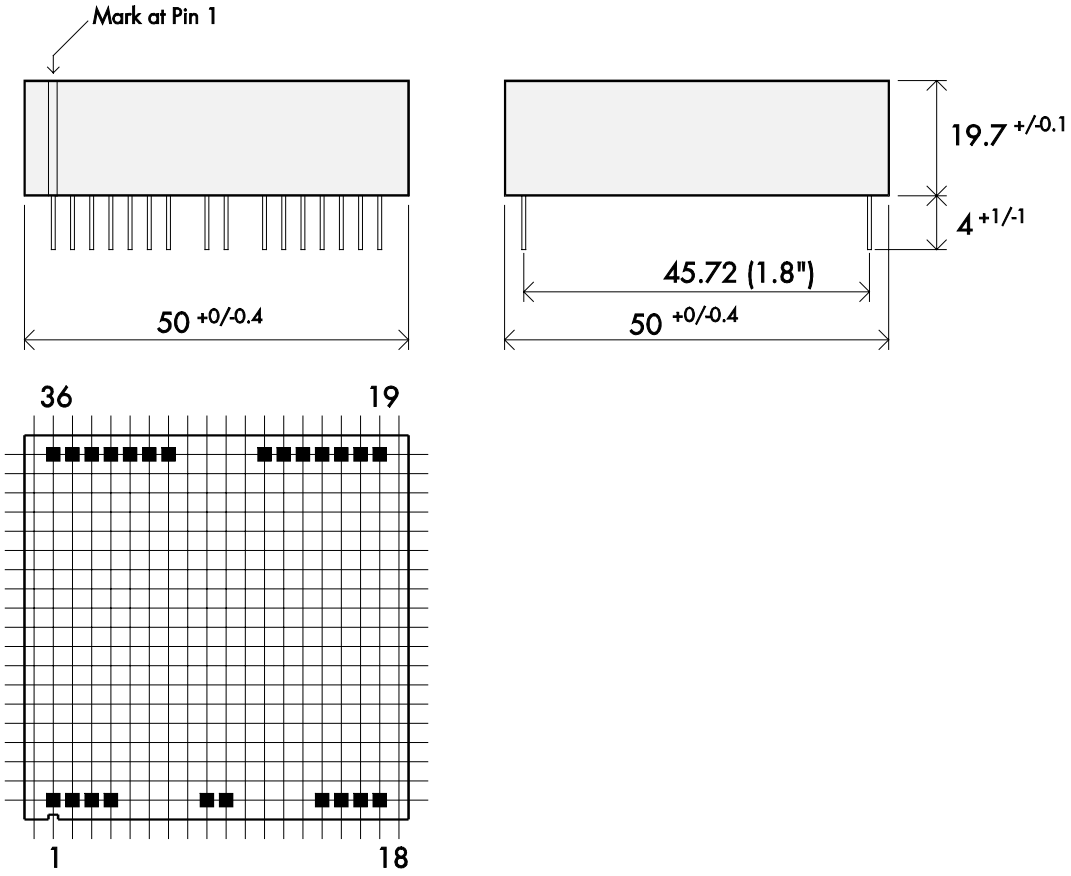


Fig. 1 Block and connection diagram of the IGD508E/IGD515E

Mechanical Dimensions



Layout overview (component side)

Grid	2.54
Solder pads	Ø 1.6
Drill holes	Ø 0.9

All dimensions are in mm

Fig. 2 Mechanical dimensions and printed circuit layout

Case & Coating

Component	Material
Case product	Noryl (PPE mod.), non-halogenate flame retardants
Coating mass	Polyurethane base, temperature-cycle resistant

General Characteristics

Quality	Standard			
Manufacturing	ISO9001 certified			
Reliability	**Standard**		**typ**	**units**
MTBF IGD508Ex	MIL HDBK 217F (see Note 12)		> 2,000,000	hours
MTBF IGD515Ex	MIL HDBK 217F (see Note 12)		> 2,000,000	hours
Thermal Characteristics	**Test Conditions**	**min**	**max**	**units**
Operating temperature	IGD5xxEN (see Note 13)	0	+70	°C
	IGD5xxEI (see Note 13)	-40	+85	°C
Storage temperature	All types	-40	+90	°C

Electrical Characteristics

Power Supply	Test Conditions	min	typ	max	units
Supply voltage V_{cc} (see Note 1)	Pin 10 to Pin 9	12	15	16	Vdc
Supply current I_{cc} (see Note 2)	Without load		50		mA
Max. supply current I_{cc}	All types (see Note 3 & 11)			450	mA
Output power DC/DC converter	All types (see Note 3 & 11)			6	W
Efficiency η	Internal DC/DC converter		85		%
Turn-on threshold V_{th}	All types		10		Vdc
Hysteresis on-/off (see Note 4)	All types		0.6		Vdc
Coupling capacitance C_{io}	All types (see Note 6)		<10		pF
Logic Inputs	**Test Conditions**	**min**	**typ**	**max**	**units**
Max. input voltage V_{in}	All types (see Note 5)			5	Vdc
Input voltage for logic "1"	All types (see Note 7)	3.8			Vdc
Input voltage for logic "0"	All types (see Note 7)			0.9	Vdc
Vce-Monitoring	**Test Conditions**	**min**	**typ**	**max**	**units**
Inputs ME	to E1/COM	-0.5		V_{cc}	Vdc

Electrical Characteristics (Continuation)

Timing Characteristics	Test Conditions	min	typ	max	units
Delay time input to output	Turn-on $t_{pd(on)}$ (see Note 14)		100		ns
	Turn-off $t_{pd(off)}$ (see Note 14)		100		ns
Delay time status output	Pin 35 (see Note 16)		75		ns

Outputs	Test Conditions	min	typ	max	units
Output current I_{out} (see Note 8)	IGD508Ex Pin 25	-8		+8	Adc
	IGD515Ex Pin 25	-15		+15	Adc
Output rise time $t_{r(out)}$ (see Note 9)	All types		40		ns
Output fall time $t_{f(out)}$ (see Note 9)	All types		40		ns
Output current SO	All types Pin 35			90	mA
Output voltage rating SO	All types Pin 35			40	V
Output current +5V	All types Pin 31			30	mA

Electrical Isolation	Test Conditions	min	typ	max	units
Operating voltage (see Note 10)	Continuous or repeated			2500	Vdc
Test voltage	(50Hz/1min) (see Note 17)			7500	Vaceff
Partial discharge extinction volt.	IEC270 (see Note 15)		2200		Veff

All data refer to +25°C and V_{cc} = 15V unless otherwise specified

Footnotes to the key data

1) At a supply voltage greater than 16V, the open-circuit voltages on the two output sides of the DC/DC converter may exceed 18V. This can lead to the destruction of the driver and protection circuits on the output side.
2) Only internal consumption of the drivers, static.
3) If the specified power consumption is exceeded, this indicates an overload of the DC/DC converter. It should be noted that these DC/DC converters are not protected against overload.
4) The turn-off threshold is lower than the turn-on threshold by the magnitude of the hysteresis. The turn-on and turn-off thresholds allow the drivers to be run at operating voltages of 12V to 15V and cannot be changed.
5) This refers to the logic inputs INPUT (Pin 32), INV (Pin 33) and SDOSA (Pin 34).
6) Coupling capacitance of the DC/DC converter.
7) Guaranteed logic level for the logic inputs INPUT (Pin 32), INV (Pin 33) and SDOSA (Pin 34), of which only INPUT (Pin 32) has a Schmitt trigger characteristic.
8) The gate current must be limited to its maximum value by a gate resistor.
9) At a load of 1 µF in series with 2 Ohm.
10) Maximum continuous or repeatedly-applied DC voltage or peak value of the repeatedly-applied AC voltage between the power supply inputs and all other terminals. However, types that have been measured and selected for higher partial-discharge voltages are also available (see Note 15).
11) The output power of the DC/DC converter is 6 W, of which about 1 W must be used for the driver's own supply and for the fiber-optic links. This leaves another 5 W for driving the power semiconductors.

However, some FOLs require even more power, in which case the power available for driving is reduced.

12) The MTBF (mean time between failures) is calculated to MIL HDBK 217F at an ambient temperature of 40°C, a typical load and when the driver is exposed to a current of air. Further information on reliability may be obtained from CONCEPT upon request.
13) The application-specific self-heating of the drivers - especially at high load - must be taken into account.
14) Transit time from Pin 32 (INPUT) to Pin 25 (G) only within the driver, without external fiber-optic links.
15) The partial discharge is not measured for the standard types. For main power applications, a sufficient safety margin exists between the typical operating voltage of < 600Vdc and the partial discharge extinction voltage of typically about 1500 Vpeak. Tested and selected types with guaranteed partial-discharge immunity can be supplied for applications with maximum requirements and higher operating voltages (such as railroad applications).
16) Transit time from a turn-on or turn-off edge of the input signal at Pin 32 (INPUT) to the first edge of the acknowledgement at Pin 35 (SO) only within the driver, without external fiber-optic links. The transit time to Pin 35 (SO) within the driver after a protection function responds is even shorter.
17) The test voltage of 7500 Vac(rms)/50Hz may be applied only once during a minute. It should be noted that with this (strictly speaking obsolete) test method, some (minor) damage occurs to the isolation layers due to the partial discharge. Consequently, this test is not performed at CONCEPT as a series test. In the case of repeated isolation tests (e.g. module test, equipment test, system test) the subsequent tests should be performed with a lower test voltage: the test voltage is reduced by 750V for each additional test. The more modern if more elaborate partial-discharge measurement is better suited than such test methods as it is almost entirely non-destructive.

Functional Description

Overview

The intelligent drivers of the IGD series are universal drive modules designed for power MOSFETs and IGBTs in switching operation. The IGD508E and IGD515E types are mutually pin-compatible and differ only in their maximum gate currents.

The IGD types with higher gate currents are eminently suited for large modules or for a number of transistors connected in parallel as well as for high-frequency applications (due to the thermal stress in the final stages).

In conjunction with a pair of fiber-optic links (FOLs), the intelligent drivers of the IGD series represent a complete solution for all driving and protection problems associated with power MOSFET and IGBT power stages. Almost no other components are required in the control circuit and in the power section.

Reliable operation

Gate driving with a positive and negative control voltage (between ±12V and ±15V depending on the selected supply voltage) allows reliable operation of IGBT modules of any size from any manufacturer. Thanks to the great interference immunity attained by means of the negative gate voltage, a number of power MOSFET or IGBT modules can be connected in parallel without the user having to worry about parasitic switching operations or oscillations.

The components contain an overcurrent and short-circuit protection circuit for the power transistors, a feed monitoring function, a status acknowledgement, a mode for brake operation, a mode for series and parallel circuits as well as an electrically-isolated supply for the drive electronics via an integrated DC/DC converter.

Genuine electrical isolation

The outstanding electrical isolation of up to 2500 V operating voltage (corresponding to a test voltage of 7500 V) between the control and power sections predestine these drive modules for applications in which large potential differences and large potential jumps occur between the power section and the control electronics.

The design of the DC/DC converter allows operation with two 1700V-IGBTs connected in series, for example. (Higher isolation voltages upon request.)

Application benefits

Reliable power stages can be realized with power MOSFETs or IGBTs within an extremely short time by using these driver modules.

The high drive power allows simple driving of the largest power semiconductor modules and parallel circuits.

The high isolation-test voltage allows high-voltage IGBTs and series-connected transistors to be driven.

The integrated DC/DC converter allows a simple power-supply concept: a single 15-V feed is sufficient to supply any (large) number of drivers.

The short transit times of the drivers of the IGD series - in conjunction with broadband fiber-optic links - also allow them to be used in high-frequency clocked power supplies, RF converters and resonance converters.

These drivers have been manufactured by CONCEPT on the basis of many years of experience in producing intelligent drivers for power MOSFETs and IGBTs and represent a further development of the drivers of the IHD series that have already been tried and tested in large quantities.

Short-circuit and overvoltage protection

One of the basic functions of the intelligent drivers of the IGD series is to ensure reliable protection of the driven power transistors against overcurrent and short circuit. The current measurement is based on determining the drain-source or collector-emitter voltage at the turned-on transistor. After a threshold defined by the user has been exceeded, the power transistor is turned off and remains blocked in this condition for a defined minimum time (in normal mode). When this time has elapsed, the transistor is released again.

This protection concept can be used to protect IGBTs simply and reliably without the need for additional components in the power path.

Layout of the terminals

The terminal pins of the drive modules in the IGD series are configured so that the layout can be kept simple. A spacing of 45 mm is maintained between the supply pins and the power potential!

Note

In the following, the abbreviation "FOL" will be used for the term "fiber-optic link". This refers to a component of an FOL connection, such as a fiber-optic transmitter, a fiber-optic receiver or the entire FOL connection consisting of the fiber-optic transmitter, fiber-optic wire and fiber-optic receiver.

Pins 1,2,3,4,9 and 10 GND and Vcc

These pins are used for the power supply of the driver module. The nominal feed voltage is between 12 V and 15 V. To ensure reliable starting of the integrated DC/DC converter, a switching-resistant and low-inductance electrolytic capacitor must be placed in the immediate vicinity of Pins 9 and 10. The capacitance of this capacitor must not be less than that of the capacitor connected to Cs (Pin 23). The current consumption of the DC/DC converter is determined by the number of driven transistors, their gate capacitance and by the clock frequency.

Thanks to the high isolation of the feed terminals with respect to all other pins, the drivers of the IGD series can be supplied by a potential of any size.

The internal turn-on thresholds are designed so that 12-V operation is also possible. This is particularly useful for operating transistors that have very high short-circuit currents at higher gate voltages (low saturation types).

It should be noted that the drivers themselves are not protected against self-overload. A short circuit between the gate and the emitter terminal, caused by a defective power semiconductor, for example, can lead to thermal destruction of the driver.

Pin 25 - Output Gate

Pin 25 is the driver output for driving the gate. Driving is from ±12 V to ±15 V, depending on the supply voltage, but also without a negative gate voltage depending on the application and the power transistors used (see description of Pin 24, COM).

The output stages of the drivers of the IGD series are very ruggedly dimensioned. The maximum permissible gate charging current is ±8 A for the IGD508Ex and ±15 A for the IGD515Ex; this allows the largest IGBT and power MOSFET modules to be driven. A number of power modules connected in parallel can also be driven directly. The charging current must be limited by an external gate resistor. It should be noted that when the gate is driven with a ± voltage, the total voltage rise (twice 12 to 15 V) must be considered.

The gate of the power transistor must be connected to Pin 25 by means of a lead of minimum length. A gate circuit with two gate resistors and a diode can be used to set the switching speeds at turn-on and at

turn-off independently of each other (see Fig. 3).

It is mandatory to connect zener diodes immediately between the gate and emitter for IGBTs (connected in anti-series). Their zener voltage must correspond exactly to the selected gate voltage (12 V to 15 V) (see Fig. 3). They prevent the gate voltage from increasing due to parasitic effects (such as the Miller effect) to a value that is higher than the rated gate voltage. An excessively high gate voltage increases the short-circuit current to an overproportional extent and can lead to destruction of the power semiconductors.

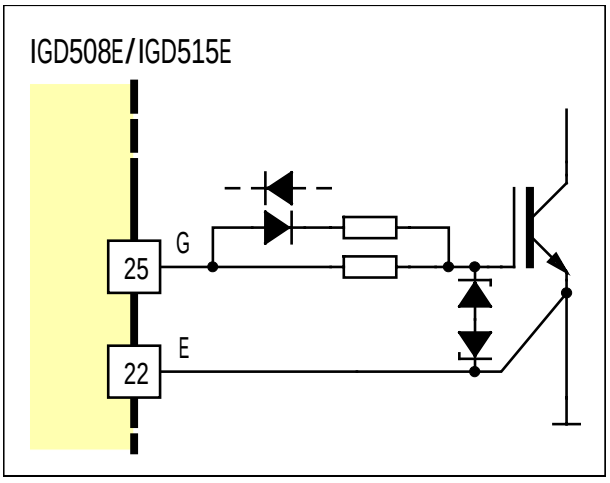


Fig. 3 Asymmetrical gate resistors

A sufficiently low-resistance termination of the gate is also ensured by the driver module when this is not supplied with the operating voltage.

Pin 22 - Emitter terminal

This pin should be connected to the emitter or source terminal of the power transistor. The connection must be as short as possible and must run directly to the emitter or source terminal of the power element. This pin should be used for modules with an auxiliary emitter or auxiliary source. It is also used as a basis for the reference, that should be connected as directly as possible to Pin 22 of the driver module.

If the connections between a driver of the IGD series and a power transistor are set up via connecting leads, then these should not exceed a length of 10 cm. The leads for the gate, emitter and the measuring pin (collector or drain terminal) should be run to each transistor in twisted form.

Pin 19 - Terminal ME

This pin is used to measure the voltage drop at the turned-on power transistor in order to ensure protection against short circuit and overload. It should be noted that it must never be connected directly to the drain or collector of the power transistor. To protect the measurement terminal from the high drain or collector voltage of the turned-off power element, a circuit with a high-blocking diode (Dme) or several diodes of the 1N4007 type connected in series should be included (see Fig. 4). It is absolutely recommended to overdimension these diodes in terms of voltage.

A pull-up resistor integrated in the driver module ensures that a current flows through the measurement diode (DMe), the attenuation resistor (Rme) and the power transistor when the latter is turned on. A potential is then present at the measurement input ME that corresponds to the forward voltage of the turned-on transistor plus the diode forward voltage and the voltage drop at Rme. Rme

attenuates the reverse-current peaks of the measurement diode Dme and should have a value of 68 Ohm.

It should be noted that the power transistors do not turn on immediately. It can take several microseconds for them to switch through fully, especially with IGBTs. Together with the integrated pull-up resistor and the external capacitor (Cme), this produces a delay in the measurement after the power transistor has switched on. This delay shall henceforth be known as the response time. This response time (and thus Cme) must be selected to be greater in inverse proportion to the speed at

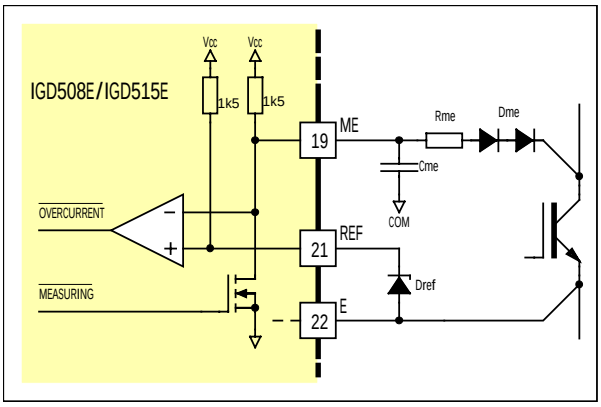


Fig. 4 Principle of V_{CE} monitoring

which the power transistors turn on. The formula for dimensioning Cme is given on page 17.

It should further be noted that negative voltages are not permissible at the measurement input.

Pin 20 - Terminal Cb

After the current monitoring circuit responds, an error message is reported via the status output SO during a defined time - known henceforth as the blocking time. In normal mode (see pin 34 (SDOSA)), the power transistor is also turned off by the intelligent driver's protection function and remains in this state during the blocking time (see Fig. 5). This function is used to protect the component from thermal overload at a continuous or repeated short circuit. The blocking time can be determined by connecting Pin 20 (Cb) to Pin 24 (COM) via a capacitor (see page 17 for the formula). The capacitance of the blocking capacitor should not exceed a value of 470 nF.

After the blocking time has elapsed, the power transistor is immediately released again.

Pin 21 - Terminal REF

An external zener diode is connected to this pin as a reference. This defines the maximum voltage drop at the turned-on power transistor at which the protective function of the drive circuit is activated.

The protection functions of the intelligent drivers of the IGD series always become active when the voltage at ME (measurement drain/collector) is higher than that at REF (see Figs. 4 & 5).

The reference potential is the emitter (or source) of the power transistor. The reference must never under any circumstances be capacitively blocked.

The reference diode should be placed as closely as possible to the driver module.

Pin 23 - Terminal Cs

A switching-resistant and low-inductance blocking capacitor (an electrolytic

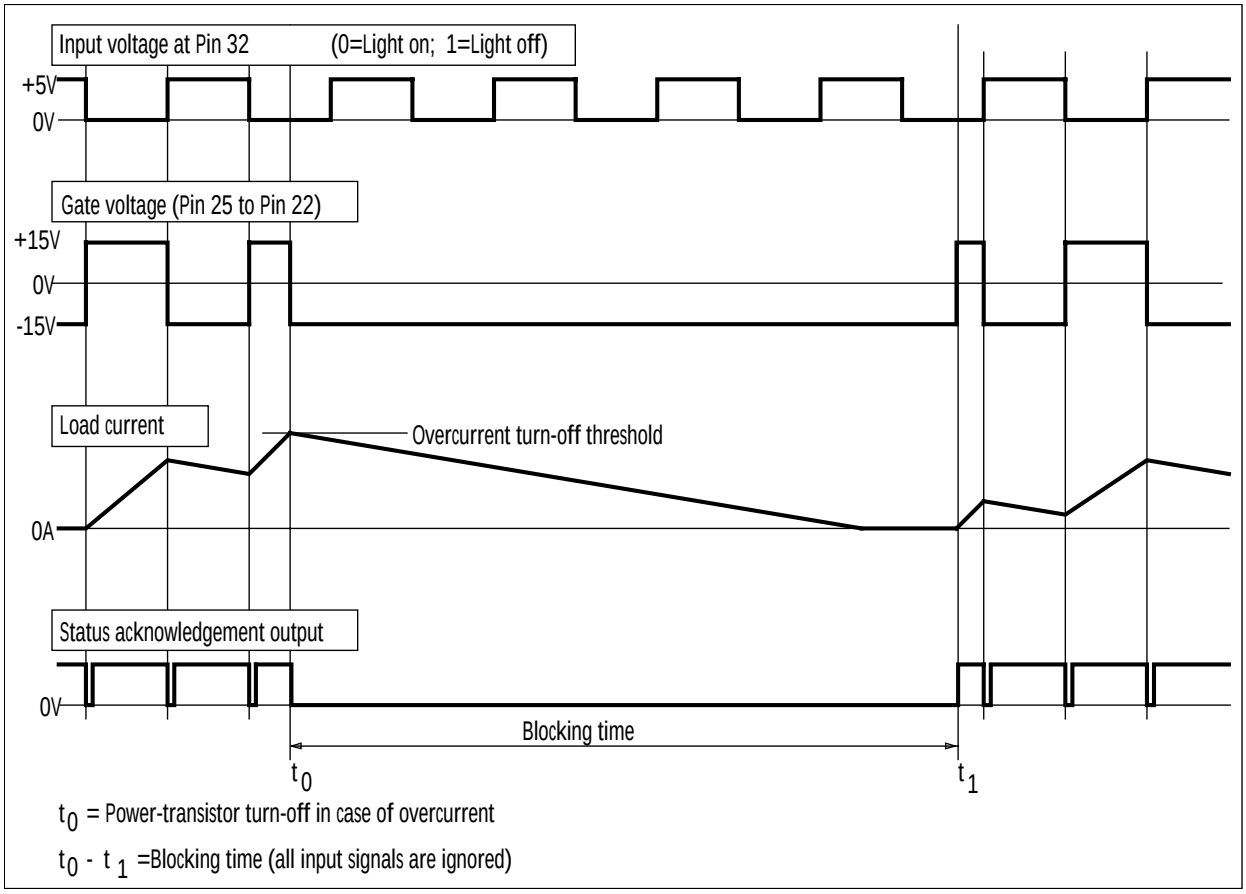


Fig. 5 Principle of the protection function and the blocking time

capacitor is usually used) is connected at this output. It decouples the DC/DC converter on the secondary side. The capacitor must supply the pulse currents (up to 8 A or 15 A) for charging the gate capacitances. The electrolytic capacitor is connected between Cs and COM. Since the charging currents for the gate capacitance are drawn mainly from this electrolytic capacitor, it must definitely be located as closely as possible to the driver module. The terminal assignment is optimally suitable for this purpose. A capacitance up to 250 mF is recommended. Significantly greater values should not be used in order to guarantee problem-free starting of the integrated DC/DC converter.

In order to prevent the operating voltage from „running up“ on the secondary side, a 16-V zener diode or a transient suppressor must be connected in parallel to the blocking capacitor. This diode should be designed for a power loss of at least 1.3 W.

Pin 24 - Terminal COM

This is the ground pin of the secondary-side blocking capacitor. It is used at the same time as the reference potential for the measuring filter and the capacitor Cb.

The COM terminal can be connected to the source of a power MOSFET in place of E. The anode of the reference diode must then also be connected to this pin. This circuit allows power MOSFETs to be

driven without a negative gate voltage. The transistor is then driven in the turned-off state with 0 V (unipolar gate driving, see Fig. 6).

The terminal E is not used in this circuit and must never under any circumstances be connected to COM.

This method of gate driving is not as a rule useful for IGBTs, as a negative gate voltage should always be used for larger modules.

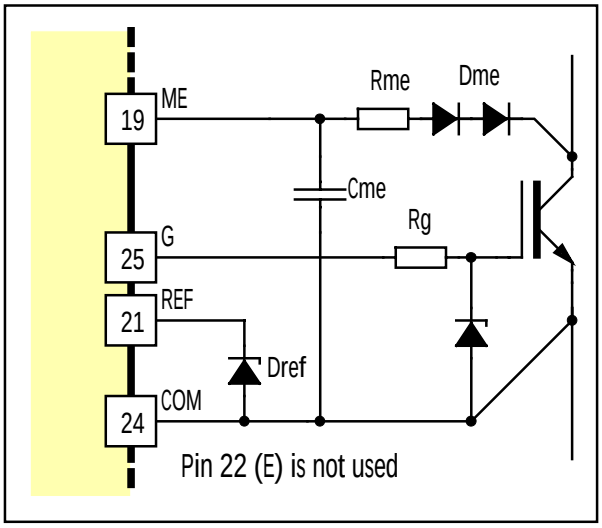


Fig. 6 Unipolar gate driving (0/+15V)

Pin 30 - Terminal IGND

This is the ground pin for the interface electronics, specifically for the FOL receiver (see Fig. 7).

Pin 31 - Terminal +5 V

A voltage of +5 V with respect to IGND is applied to this pin. It is designed to supply the interface electronics, specifically the FOL receiver (see Fig. 7). The maximum current of 30 mA for this output must not be exceeded. Most receivers require less current. If an FOL receiver that requires more than 30 mA is used, then an external 5-V controller should be connected. It can be supplied by Pin 23 (Cs).

Pin 32 - Terminal INPUT

The output signal of the FOL receiver is applied to this input (see Fig. 7). In principle, this component may be obtained from any manufacturer. For high-quality applications, however, suitable FOL products should be used; CONCEPT is happy to advise its customers on this point. Examples of suitable FOL receivers are: HFBR2521 and HFBR2522 (from Hewlett-Packard) as well as SFH551V and SFH551/1V (from Siemens).

As the familiar FOL receivers supply a 0 V signal when the drive information is applied (i.e. when current flows through the FOL receive diode), this input is suitably designed. A 5-V signal corresponds to the status of „power semiconductor turned off“; a 0-V signal to that of „power semiconductor turned on“. However, the latter output status is possible only when the protection function has not responded in normal mode (see Pin 34, SDOSA).

The INPUT terminal has a Schmitt trigger characteristic in order to attain a high signal-to-noise ratio.

The logic function of the INPUT terminal can also be inverted by Pin 33 (INV).

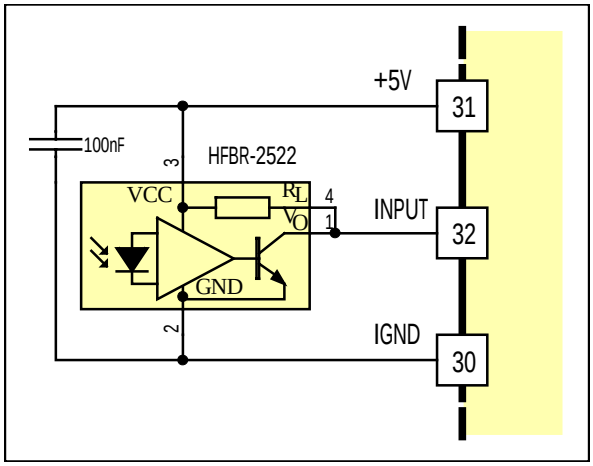


Fig. 7 Fiber-optic receiver wiring

Pin 33 - Terminal INV

This pin allows the input signal INPUT to be inverted. This input is normally connected to IGND. A 5-V signal at the INPUT terminal then corresponds to the status of „power transistor turned off“ and a 0-V signal to that of „power transistor turned on“. If INV is connected to +5 V, then precisely the opposite is true.

The input INV allows connection of an FOL receiver with a „high“ or „low“ output signal in the driven status.

However, this function is used particularly frequently in drives with brake choppers. The status of „current in the FOL transmit diode“ then means „brake chopper turned off“. Turn-off or absence of the drive signal then activates the brake.

Pin 34 - Terminal SDOSA

This pin is used for mode selection and affects the reaction of the protection function.

In normal operation, the SDOSA terminal (Pin 34) remains open. This has the effect that when a fault (in the desaturation or supply-voltage monitoring circuits) occurs, the power semiconductor is immediately turned off, even if the input signal continues to be applied. The fault status is simultaneously reported to the control electronics via the status output SO.

The second operating mode is designed specifically for the series connection of power MOSFETs and IGBTs. For this mode, the SDOSA input is connected to +5 V. This now has the effect that when an error (in the desaturation or supply-voltage monitoring circuits) occurs, the power semiconductor is not turned off. The status output SO merely reports the error status to the control electronics, which must now centrally turn off all the drivers simultaneously as quickly as possible. This is the only way of ensuring the symmetry in the series circuit even if a protective function is triggered.

The same function can also be used if several power semiconductor modules are connected in parallel, each with a separate driver. In this case, the symmetry of the current distribution is retained by the simultaneous turn-off of the drivers.

The driver thus allows any combination of series and parallel circuits of power MOSFETs or IGBTs.

This function can also be used in bridge circuits, for example to ensure that all power semiconductors are turned off simultaneously in the case of a fault.

In each of these cases it is important that linking the status acknowledgements in the event of a fault produces a turn-off of all drive pulses as quickly and directly as possible. The term direct here refers to the signal path: the linkage should be

realized within a single PAL or FPGA and not by a complex circuit structure or a microprocessor. FPGAs with suitable programming may be obtained from CONCEPT upon request.

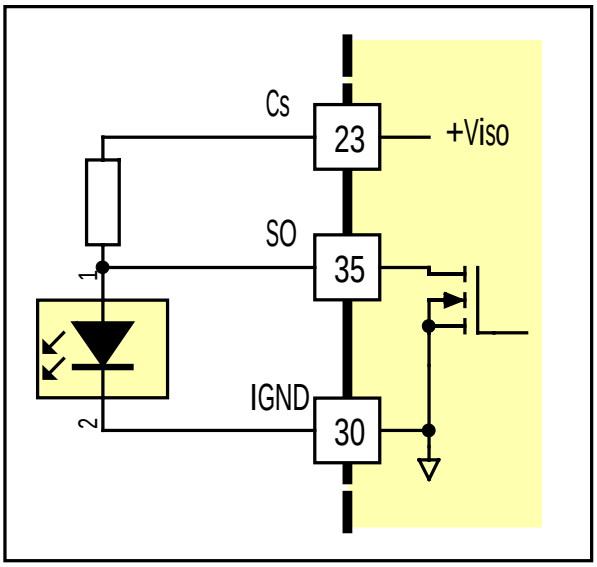


Fig. 8 Fiber-optic transmitter wiring

Pin 35 - Terminal SO

This is the status output of the driver. An FOL transmitter for the status acknowledgement is connected to it via a dropping resistor (see Fig. 8). The supply voltage should be obtained from Pin 23 (Cs). A voltage of about +15 V is present here.

The status output SO has the following statuses:

If the supply voltage is too low, then the FET at output SO is through-connected. This means that no current flows through the FOL transmitter.

If the supply voltage - but no error status - is applied, then the output SO is high-impedance. This means that a current flows through the FOL transmitter of the status acknowledgement circuit.

After the protection function (desaturation monitoring) of the driver has detected an error status, the output SO is through-connected for the duration of the blocking time. The error status is thus reported to the control electronics (see Fig. 5)

This output also acknowledges every switching edge of the driving signal with a short pulse, during which the FET becomes conducting (see Fig. 5). The length of the acknowledgement pulse is determined by connecting Pin 36 (Cq) to a capacitor.

The acknowledgement function allows the control electronics to monitor the operation of both FOL connections (i.e. the drive wire and the status acknowledgement) as well as the driver.

If the acknowledgement pulse fails to appear, then the FOL drive connection has probably failed. FOL connections that are incorrectly plugged in and transmit diodes whose luminous power is greatly reduced due to degradation effects often show the following extremely dangerous effect: the receiver emits a high-frequency noise signal in the megahertz range. This leads to thermal destruction of a power semiconductor and possibly also of the driver within microseconds. An acknowledgement pulse is then present at the SO output with every edge of the input signal. A defective status can be detected by a suitable logic circuit in the control electronics and the system can be turned off. CONCEPT can supply FPGAs with these functions upon request.

It is further recommended that the status acknowledgements are not connected together in the form of a summed

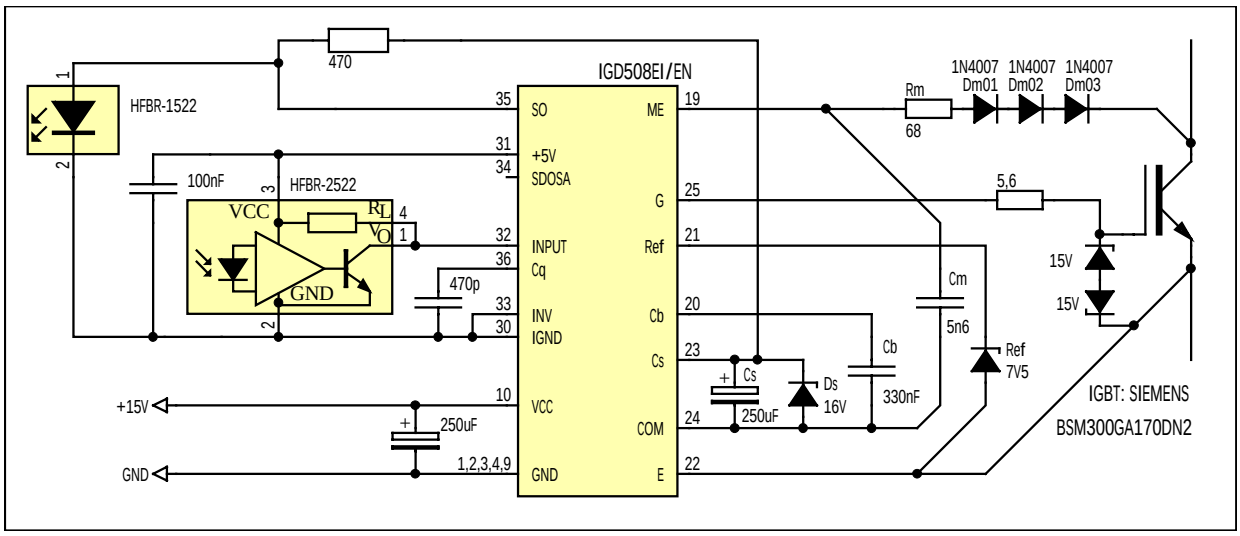


Fig. 9 Application example: Driving a 1700V/300A IGBT with IGD508Ex

message, but are evaluated as individual signals in a monitoring logic circuit. This significantly simplifies diagnosis and troubleshooting in the event of a fault.

Pin 36 - Terminal Cq

The length of the acknowledgement pulse at the output SO is determined by a capacitor at this terminal connected to Pin 24 (COM). The length of this pulse can then be optimally determined for each application (depending on the throughput rate of the FOL connections and the clock frequency). A capacitor of 470 pF at terminal Cq produces an acknowledgement pulse of about 1 µs.

If no capacitor is connected to terminal Cq, then the acknowledgement pulse is only about 30 ns in duration. Unless the FOL connection in the status acknowledgement circuit is extraordinarily fast, an acknowledgement signal is no longer visible at the receiver. This operating mode can be selected when monitoring of the FOL connection is not desired. In principle, however, operation is recommended with the acknowledgement monitoring function.

Configuration of the power section

The intelligent drivers should be placed as closely as possible to the power transistors. The connection leads to the transistors should be as short as possible, i.e. not more than 3 to 10 cm in length depending on the gate current and switching speed. In contrast, the FOL input leads can be of practically any desired length.

Application example with a 1700 V/300 A IGBT

Fig. 9 shows an example circuit with a BSM300GA170DN2 from SIEMENS. The optical-waveguide components HFBR-1522 and HFBR-2522 are from Hewlett-Packard. Pin 34 (SDOSA) is open, so the driver is in normal operation. This means that it turns the IGBT off in the event of a fault. Pin 33 (INV) is on ground, so the signal transfer is non-inverting. The capacitor at Pin 36 (Cq) generates acknowledgement pulses of about 1 µs. The response time with Cme=5n6 and Ref=7V5 is about 7 µs. The response threshold is about twice the rated current.

This example should give you some initial idea. The exact dimensioning should be checked critically in every application.

Evaluation boards

Completely assembled and tested multiphase IGBT inverter bridges from 10 kW to about 1 MW are currently available.

In conjunction with the documentation, these boards can be used to set up operational prototype equipment within a matter of hours.

Formulas for Circuit Calculations

Response Time Capacitor

$$C_{me} = \frac{t_a}{1{,}5k\Omega \ \ln\left(\frac{V_{cc}}{V_{cc} - V_{ref}}\right)}$$

Blocking Time Capacitor

at ±15V gate driving

$$C_b = \frac{t_b}{71{,}6k\Omega}$$

$C_{b\,max}$ = 470nF

at unipolar gate driving (=/+15V)

$$C_b = \frac{t_b}{100k\Omega \ \ln\left(\frac{2 \cdot V_{cc}}{V_{ref}}\right)}$$

$C_{b\,max}$ = 470nF

Supplementary Services

CONCEPT makes the practical experience gained over many years by its development and application engineers available to all interested users. CONCEPT offers various services within the scope of this offer:

Consulting and Training

CONCEPT provides consulting and training services to customers on optimal procedures, the ideal circuit topology and the avoidance of possible difficulties in the development of power electronics.

Technical Support

CONCEPT offers you fast and effective help for your questions and problems:

E-Mail: concept@bielstar.ch

Tel ++41 (0)32 / 322 42 36
Fax ++41 (0)32 / 322 22 51

Application

CONCEPT calculates and dimensions power sections and driver circuits according to the customer's specifications and supplies complete circuit diagrams, parts lists and electrical and thermal key data of the circuit. The customer then implements the layout and construction of the equipment himself.

Customer-Specific Systems

CONCEPT develops and produces complete equipment and systems according to the customer's specifications.

Quality

The obligation to high quality is one of the central features laid down in the mission statement of CT-Concept Technology Ltd. Total Quality Management (TQM) covers all stages of product development and production up to delivery. The drivers of the IHD series are manufactured according to the ISO9001 quality standard.

Exclusion Clause

CONCEPT reserves the right to make modifications to its technical data and product specifications at any time without prior notice. The general terms and conditions of delivery of CT-Concept Technology Ltd. apply.

Fax Reply Form

Please use a photocopier to enlarge to A4 size. Check relevant box [✘]. Please complete the form and fax it to CONCEPT or to your local CONCEPT distribution partner!

Please send us further information:

❑ Overview of all intelligent drivers from CONCEPT
❑ Overview of the evaluation boards

We would like a quotation for:

❑ _____ pcs intelligent drivers of type IGD _____, by date:_____
❑ _____ pcs intelligent drivers of type IGD _____, by date:_____
❑ _____ pcs intelligent drivers of type IGD _____, by date:_____

We would be interested in the following services:

(See description in the data sheet)

❑ Troubleshooting and support for technical problems
❑ Application (dimensioning of power stages)
❑ Customer-specific systems

My address:

Forename, Surname

Department/Function

Company

Telephone Fax

E-Mail

Our business activities are in the sector of

Ordering Information

Drivers for ±8A gate current

Standard version (0...70°C)	IGD 508 EN
Industry version (-40...+85°C)	IGD 508 EI

Drivers for ±15A gate current

Standard version (0...70°C)	IGD 515 EN
Industry version (-40...+85°C)	IGD 515 EI

Other Products and Information

Drivers for higher isolation voltages (i.e. railroad applications)

Please request further information

Other intelligent drivers (i.e. half-bridge drivers etc.)

Please ask for an "Overview of intelligent drivers"

Evaluation boards

Please ask for an "Overview of evaluation boards"

Manufacturer Your Distribution Partner

CT-Concept Technology Ltd.
Intelligent Power Electronics
Hauptstrasse 3
CH-2533 Leubringen / Evilard
(Switzerland)

Tel ++41 (0)32 / 322 42 36
Fax ++41 (0)32 / 322 22 51