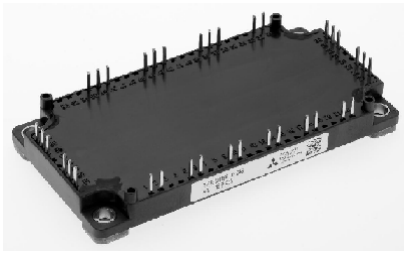
CM75TX-24S

HIGH POWER SWITCHING USE
INSULATED TYPE

CM75TX-24S



sixpack (3φ inverter)

- 6th Generation NX series -

Collector current I_C ..... **75** A

Collector-emitter voltage V_{CES} ..... **1200** V

Maximum junction temperature T_{jmax} ... **175** °C

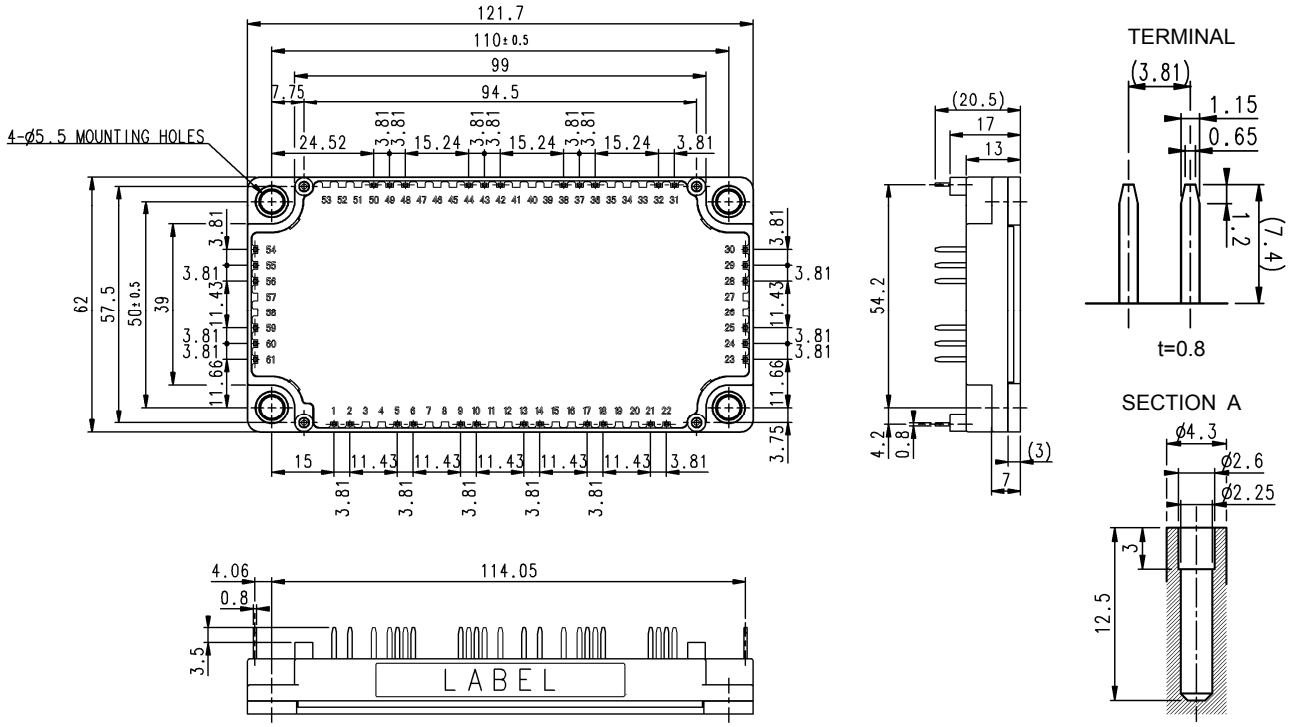
- ●Flat base Type
- ●Copper base plate (non-plating)
- ●Tin plating pin terminals
- ●RoHS Directive compliant
- ●UL Recognized under UL1557, File E323585

APPLICATION

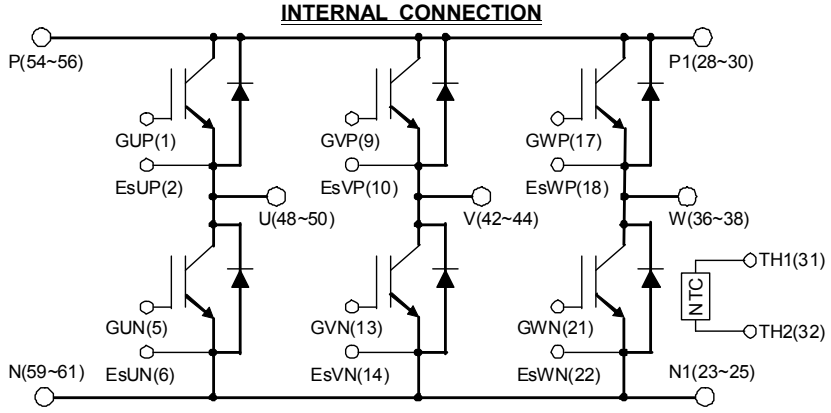
AC Motor Control, Motion/Servo Control, Power supply, etc.

OUTLINE DRAWING & INTERNAL CONNECTION

Dimension in mm



INTERNAL CONNECTION



Caution: Each (three) pin terminal of P/N/P1/N1/U/V/W is connected in the module, but should use all each three pins for the external wiring.

Tolerance otherwise specified

Division of Dimension		Tolerance
0.5	to 3	±0.2
over 3	to 6	±0.3
over 6	to 30	±0.5
over 30	to 120	±0.8
over 120	to 400	±1.2

The tolerance of size between terminals is assumed to be ±0.4.

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_j=25 °C, unless otherwise specified)

Inverter part IGBT/FWDi

Symbol	Item	Conditions	Rating	Unit
V_{CES}	Collector-emitter voltage	G-E short-circuited	1200	V
V_{GES}	Gate-emitter voltage	C-E short-circuited	±20	V
I_C	Collector current	DC, T_C=122 °C (Note.2)	75	A
I_{CRM}		Pulse (Note.3)	150	
P_{tot}	Total power dissipation	T_C=25 °C (Note.2, 4)	600	W
I_E (Note.1)	Emitter current	T_C=25 °C (Note.2, 4)	75	A
I_{ERM} (Note.1)		Pulse (Note.3)	150	

Module

Symbol	Item	Conditions	Rating	Unit
T_{jmax}	Maximum junction temperature	-	175	°C
T_{Cmax}	Maximum case temperature	(Note.2)	125	
T_{jop}	Operating junction temperature	-	-40 ~ +150	°C
T_{stg}	Storage temperature	-	-40 ~ +125	
V_{isol}	Isolation voltage	Terminals to base plate, RMS, f=60 Hz, AC 1 min	2500	V

ELECTRICAL CHARACTERISTICS (T_j=25 °C, unless otherwise specified)

Inverter part IGBT/FWDi

Symbol	Item	Conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}, G-E short-circuited		-	-	1	mA
I_{GES}	Gate-emitter leakage current	V_{GE}=V_{GES}, C-E short-circuited		-	-	0.5	μA
$V_{GE(th)}$	Gate-emitter threshold voltage	I_C=7.5 mA, V_{CE}=10 V		5.4	6.0	6.6	V
V_{CEsat} (Terminal)	Collector-emitter saturation voltage	I_C=75 A (Note.5), V_{GE}=15 V	T_j=25 °C	-	1.80	2.25	V
			T_j=125 °C	-	2.00	-	
			T_j=150 °C	-	2.05	-	
V_{CEsat} (Chip)	Collector-emitter saturation voltage	I_C=75 A (Note.5), V_{GE}=15 V	T_j=25 °C	-	1.70	2.15	V
			T_j=125 °C	-	1.90	-	
			T_j=150 °C	-	1.95	-	
C_{ies}	Input capacitance	V_{CE}=10 V, G-E short-circuited		-	-	7.5	nF
C_{oes}	Output capacitance			-	-	1.5	
C_{res}	Reverse transfer capacitance			-	-	0.13	
Q_G	Gate charge	V_{CC}=600 V, I_C=75 A, V_{GE}=15 V		-	175	-	nC
$t_{d(on)}$	Turn-on delay time	V_{CC}=600 V, I_C=75 A, V_{GE}=±15 V, R_G=8.2 Ω, Inductive load		-	-	300	ns
t_r	Rise time			-	-	200	
$t_{d(off)}$	Turn-off delay time			-	-	600	
t_f	Fall time			-	-	300	
V_{EC} (Note.1) (Terminal)	Emitter-collector voltage	I_E=75 A (Note.5), G-E short-circuited	T_j=25 °C	-	1.8	2.25	V
			T_j=125 °C	-	1.8	-	
			T_j=150 °C	-	1.8	-	
V_{EC} (Note.1) (Chip)	Emitter-collector voltage	I_E=75 A (Note.5), G-E short-circuited	T_j=25 °C	-	1.7	2.15	V
			T_j=125 °C	-	1.7	-	
			T_j=150 °C	-	1.7	-	
t_{rr} (Note.1)	Reverse recovery time	V_{CC}=600 V, I_E=75 A, V_{GE}=±15 V, R_G=8.2 Ω, Inductive load		-	-	300	ns
Q_{rr} (Note.1)	Reverse recovery charge			-	4.0	-	μC
E_{on}	Turn-on switching energy per pulse	V_{CC}=600 V, I_C=I_E=75 A, V_{GE}=±15 V, R_G=8.2 Ω, T_j=150 °C, Inductive load		-	7.3	-	mJ
E_{off}	Turn-off switching energy per pulse			-	8.0	-	
E_{rr} (Note.1)	Reverse recovery energy per pulse			-	6.9	-	mJ
$R_{CC'+EE'}$	Internal lead resistance	Main terminals-chip, per switch, T_C=25 °C (Note.2)		-	-	2.4	mΩ
r_g	Internal gate resistance	Per switch		-	0	-	Ω

ELECTRICAL CHARACTERISTICS (cont.; T_j=25 °C, unless otherwise specified)

NTC thermistor part

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
R_{25}	Zero power resistance	T_C=25 °C (Note.2)	4.85	5.00	5.15	kΩ
ΔR/R	Deviation of resistance	T_C=100 °C, R_{100}=493 Ω	-7.3	-	+7.8	%
$B_{(25/50)}$	B constant	Approximate by equation (Note.6)	-	3375	-	K
P_{25}	Power dissipation	T_C=25 °C (Note.2)	-	-	10	mW

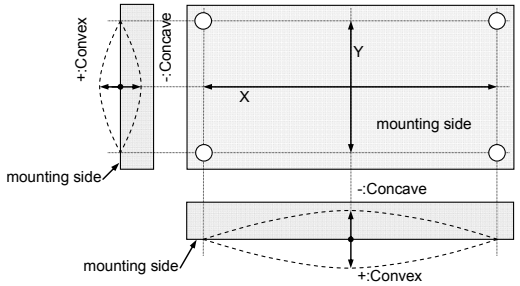
THERMAL RESISTANCE CHARACTERISTICS

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Thermal resistance (Note. 2)	Junction to case, per IGBT	-	-	0.25	K/W
$R_{th(j-c)D}$		Junction to case, per FWDi	-	-	0.40	
$R_{th(c-s)}$	Contact thermal resistance (Note.2)	Case to heat sink, per 1 module, Thermal grease applied (Note.7)	-	15	-	K/kW

MECHANICAL CHARACTERISTICS

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
M_s	Mounting torque	Mounting to heat sink M 5 screw	2.5	3.0	3.5	N·m
d_s	Creepage distance	Terminal to terminal	10.28	-	-	mm
		Terminal to base plate	14.27	-	-	
d_a	Clearance	Terminal to terminal	10.28	-	-	mm
		Terminal to base plate	12.33	-	-	
m	Weight	-	-	300	-	g
e_c	Flatness of base plate	On the centerline X, Y (Note.8)	±0	-	+100	μm

Note.1: Represent ratings and characteristics of the anti-parallel, emitter-collector free wheeling diode (FWDi).
Note.2: Case temperature (T_C) and heat sink temperature (T_s) are defined on the each surface (mounting side) of base plate and heat sink just under the chips. Refer to the figure of chip location.
The heat sink thermal resistance should measure just under the chips.
Note.3: Pulse width and repetition rate should be such that the device junction temperature (T_j) dose not exceed T_{jmax} rating.
Note.4: Junction temperature (T_j) should not increase beyond T_{jmax} rating.
Note.5: Pulse width and repetition rate should be such as to cause negligible temperature rise.
(Refer to the figure of test circuit for V_{CEsat}, V_{EC}.)
Note.6: $B_{(25/50)} = \ln(\frac{R_{25}}{R_{50}}) / (\frac{1}{T_{25}} - \frac{1}{T_{50}})$,
R_{25}: resistance at absolute temperature T_{25} [K]; T_{25}=25 [°C]+273.15=298.15 [K]
R_{50}: resistance at absolute temperature T_{50} [K]; T_{50}=50 [°C]+273.15=323.15 [K]
Note.7: Typical value is measured by using thermally conductive grease of λ=0.9 W/(m·K).
Note.8: The base plate (mounting side) flatness measurement points (X, Y) are as follows of the following figure.



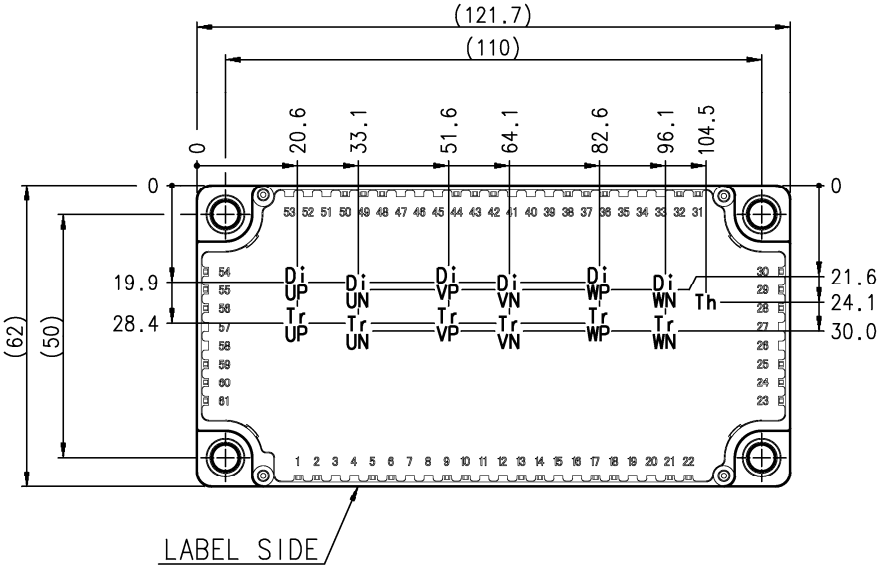
Note.9: Japan Electronics and Information Technology Industries Association (JEITA) standards,
"EIAJ ED-4701/300: Environmental and endurance test methods for semiconductor devices (Stress test I)"
Note.10: Use the following screws when mounting the printed circuit board (PCB) on the stand offs.
"M2.6×10 or M2.6×12 self tapping screw"
The length of the screw depends on the thickness of the PCB.

RECOMMENDED OPERATING CONDITIONS (T_a=25 °C, unless otherwise specified)

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	DC supply voltage	Applied across P-N / P1-N1 terminals	-	600	850	V
V_{GEon}	Gate (-emitter drive) voltage	Applied across G*P-Es*P / G*N-Es*N terminals	13.5	15.0	16.5	V
R_G	External gate resistance	Per switch	8.2	-	82	Ω

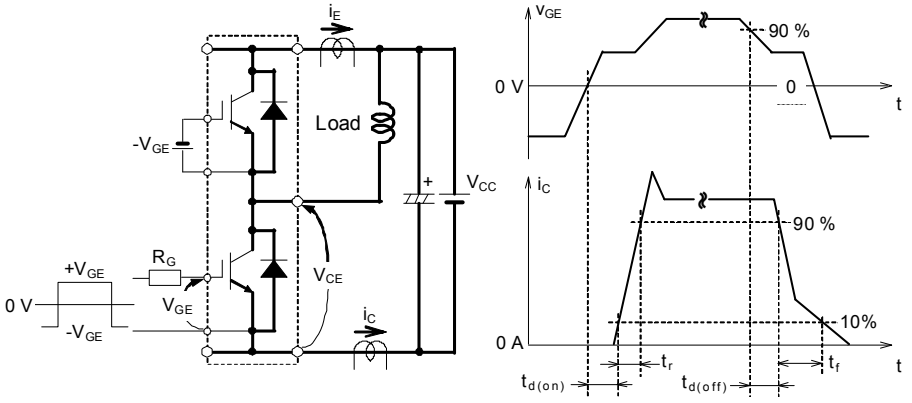
CHIP LOCATION (top view)

Dimension in mm, Tolerance: ±1 mm

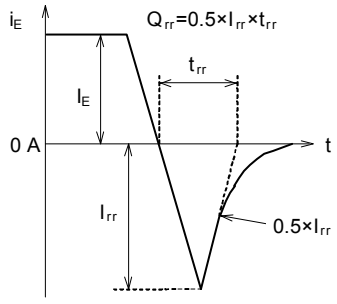


Tr*P/Tr*N: IGBT, Di*P/Di*N: FWDi, Th: NTC thermistor. Each mark points the center position of each chip.

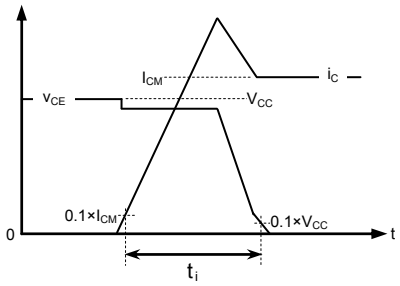
TEST CIRCUIT AND WAVEFORMS



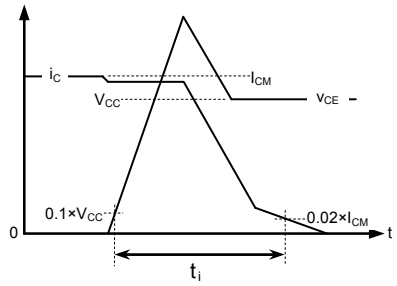
Switching characteristics test circuit and waveforms



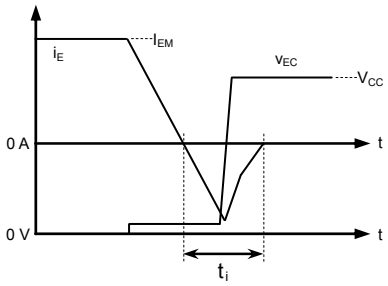
t_{rr}, Q_{rr} test waveform



IGBT Turn-on switching energy



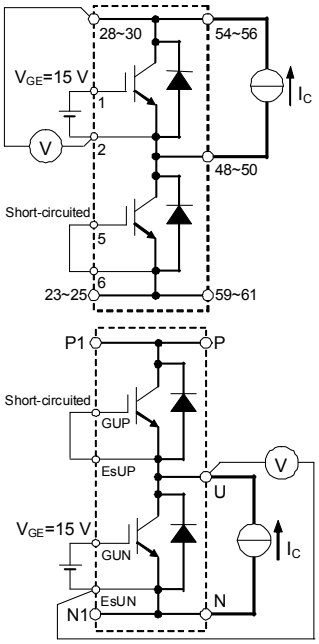
IGBT Turn-off switching energy



FWDi reverse recovery energy

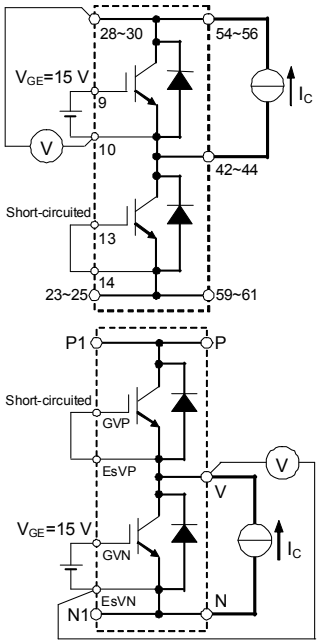
Turn-on / Turn-off switching energy and Reverse recovery energy test waveforms (Integral time instruction drawing)

TEST CIRCUIT



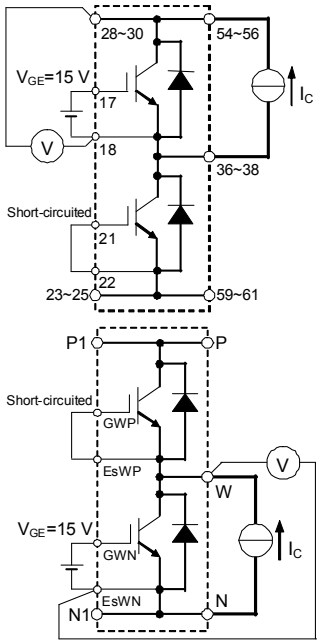
Gate-emitter short-circuited: GVP-EsVP, GWP-EsWP, GVN-EsVN, GWN-EsWN

UP / UN IGBT



Gate-emitter short-circuited: GUP-EsUP, GWP-EsWP, GUN-EsUN, GWN-EsWN

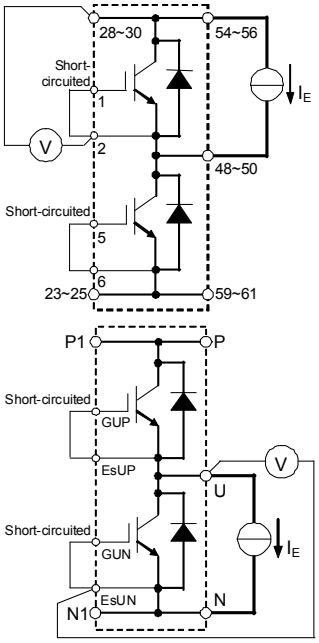
VP / VN IGBT



Gate-emitter short-circuited: GUP-EsUP, GVP-EsVP, GUN-EsUN, GVN-EsVN

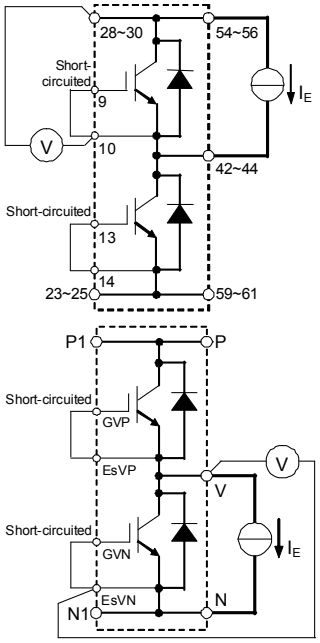
WP / WN IGBT

V_{CEsat} TEST CIRCUIT



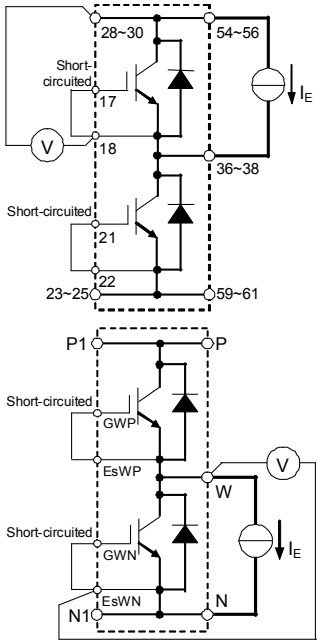
Gate-emitter short-circuited: GVP-EsVP, GWP-EsWP, GVN-EsVN, GWN-EsWN

UP / UN FWDi



Gate-emitter short-circuited: GUP-EsUP, GWP-EsWP, GUN-EsUN, GWN-EsWN

VP / VN FWDi



Gate-emitter short-circuited: GUP-EsUP, GVP-EsVP, GUN-EsUN, GVN-EsVN

WP / WN FWDi

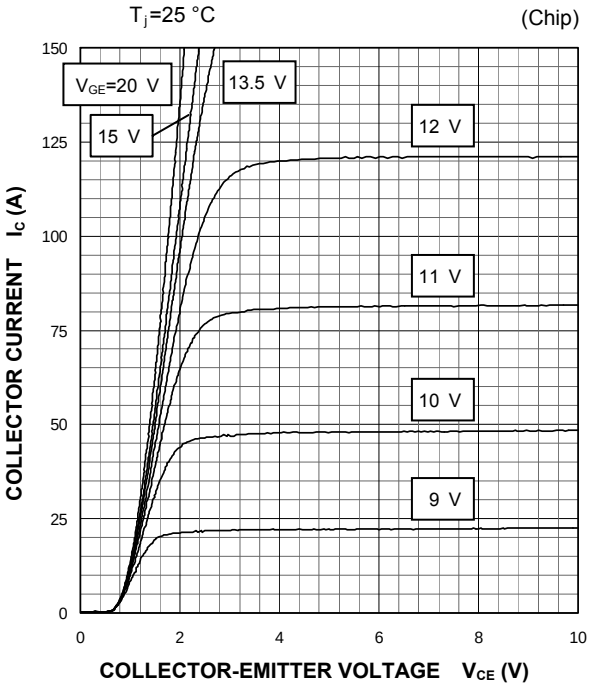
V_{EC} TEST CIRCUIT

* In the above test circuit, should use all three main pin terminals (P/N/U/V/W) for connection with the terminals and the current source.

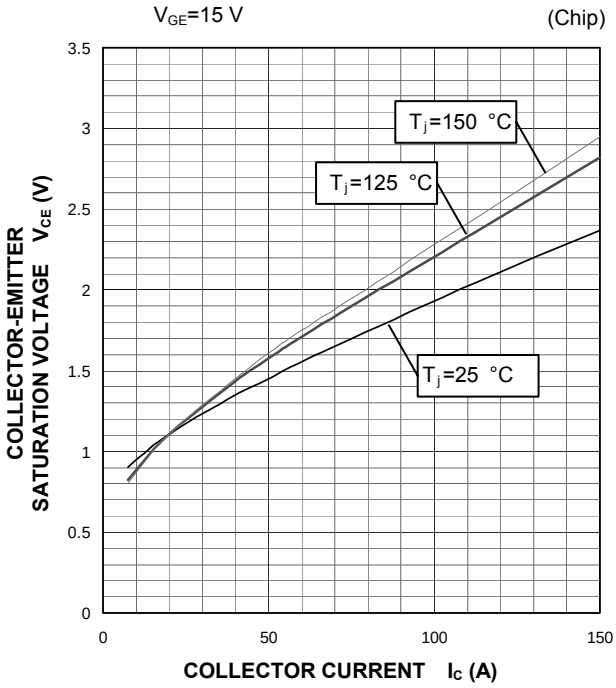
PERFORMANCE CURVES

INVERTER PART

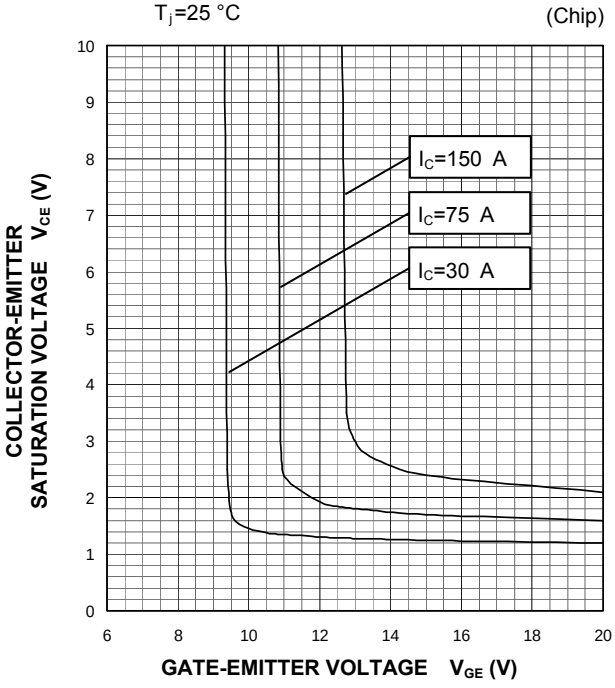
OUTPUT CHARACTERISTICS (TYPICAL)



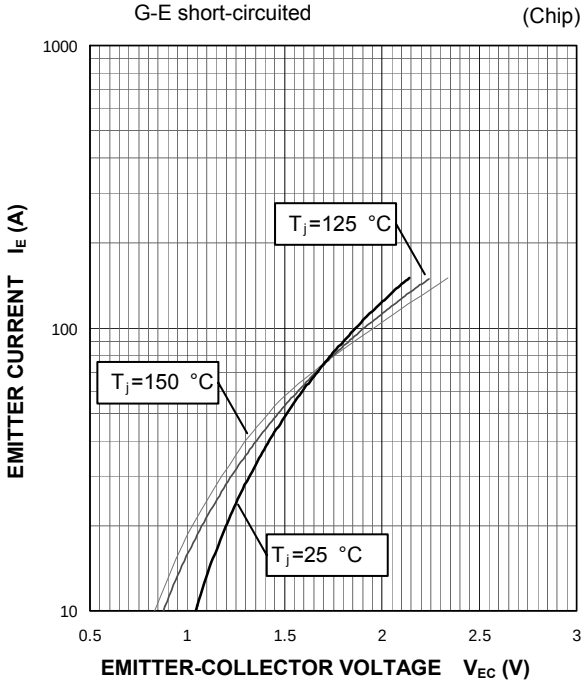
COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)



COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTIC (TYPICAL)

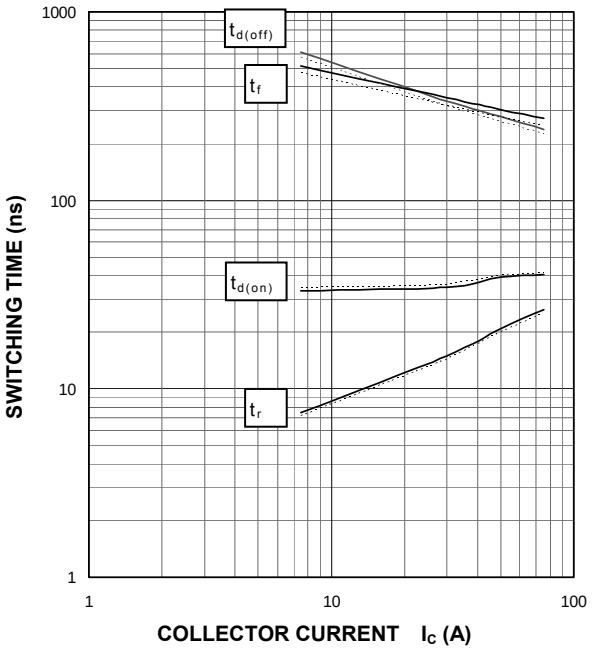


FREE WHEELING DIODE FORWARD CHARACTERISTICS (TYPICAL)



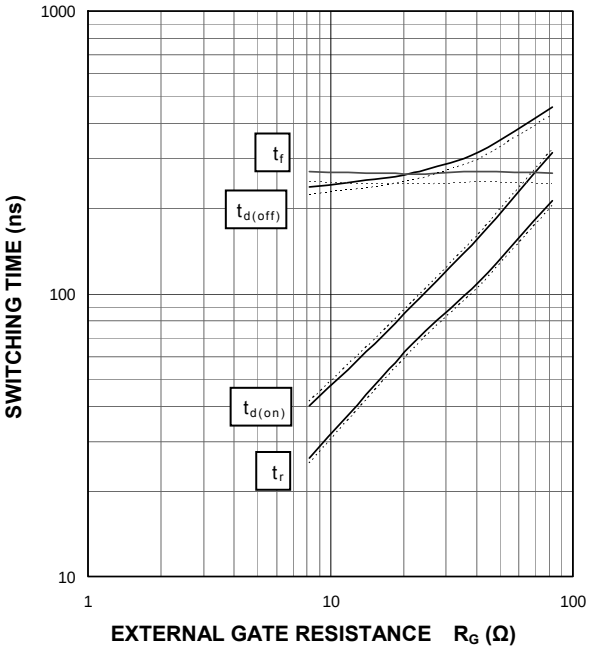
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{CC}=600 V, V_{GE}=±15 V, R_G=8.2 Ω,
——————: T_j=150 °C, - - - - -: T_j=125 °C



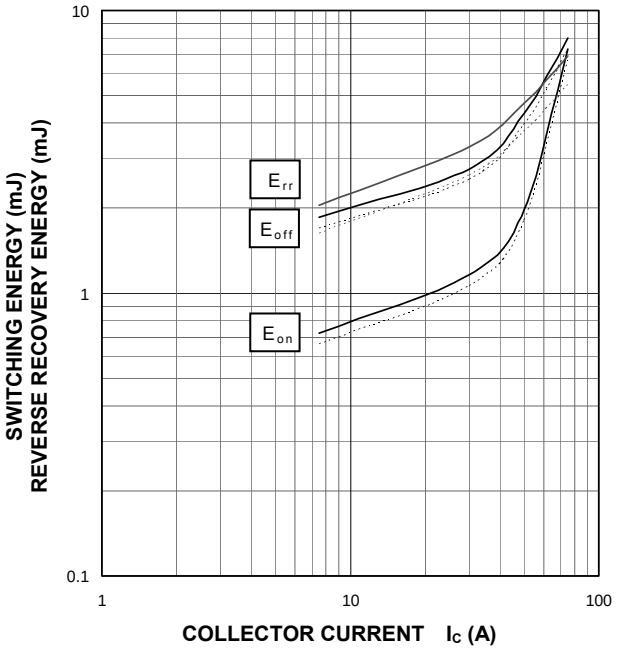
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{CC}=600 V, V_{GE}=±15 V, I_C=75 A,
——————: T_j=150 °C, - - - - -: T_j=125 °C



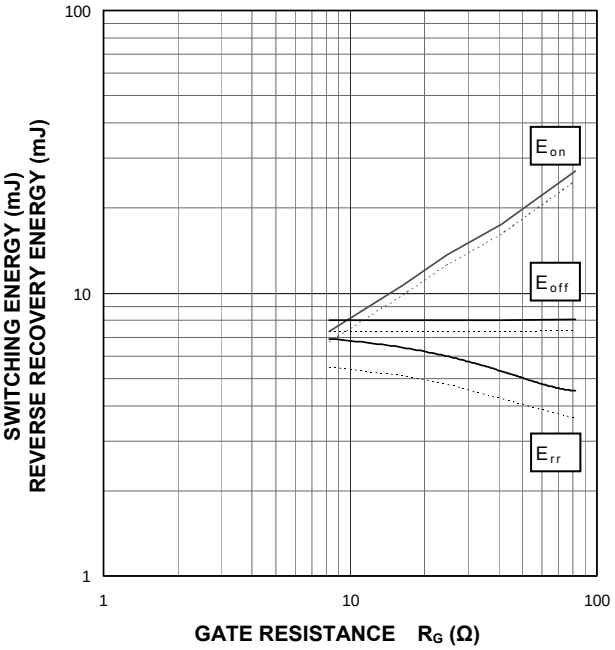
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{CC}=600 V, V_{GE}=±15 V, R_G=8.2 Ω,
——————: T_j=150 °C, - - - - -: T_j=125 °C



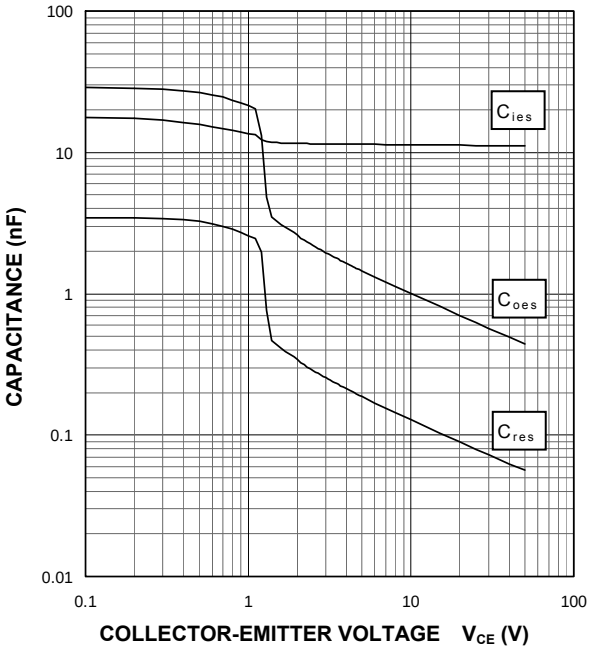
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{CC}=600 V, V_{GE}=±15 V, I_C=75 A,
——————: T_j=150 °C, - - - - -: T_j=125 °C



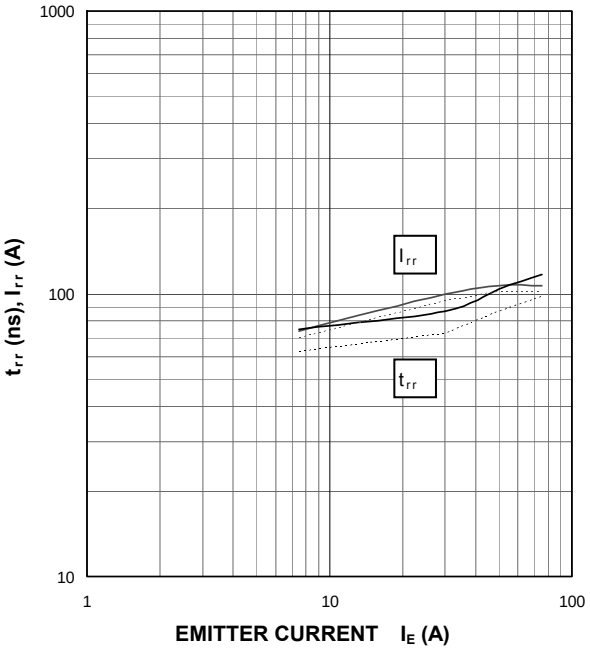
CAPACITANCE CHARACTERISTICS (TYPICAL)

G-E short-circuited, T_j=25 °C



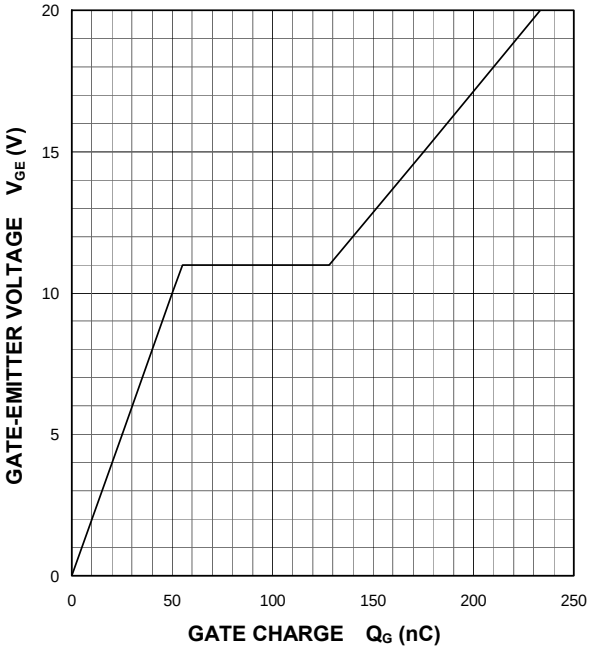
FREE WHEELING DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)

V_{CC}=600 V, V_{GE}=±15 V, R_G=8.2 Ω,
——————: T_j=150 °C, - - - - -: T_j=125 °C



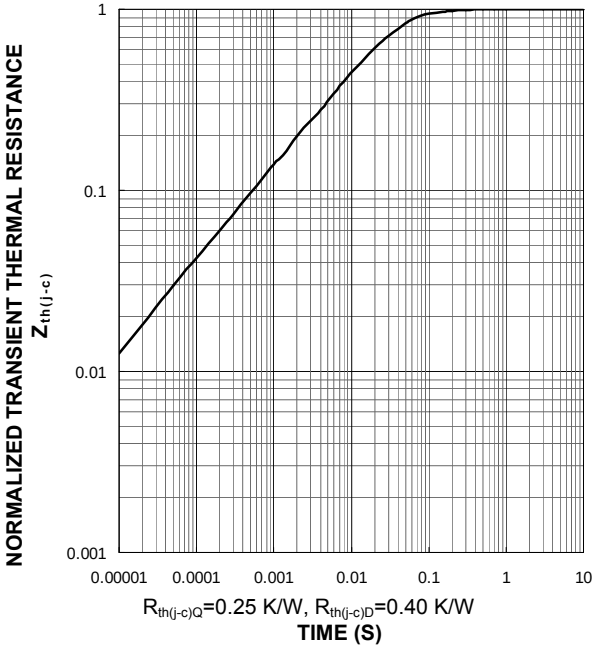
GATE CHARGE CHARACTERISTICS (TYPICAL)

V_{CC}=600 V, I_C=75 A, T_j=25 °C



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (MAXIMUM)

Single pulse, T_C=25 °C



$R_{th(j-c)Q}$=0.25 K/W, $R_{th(j-c)D}$=0.40 K/W

Keep safety first in your circuit designs!

· Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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